

## CLAIM AMENDMENTS

1           1. (currently amended) A spread spectrum digital  
2     communication receiver, the receiver comprising: [[-]]  
3           an input memory buffer [[(16)]] for storing samples of an  
4     input signal [[(y(k))]]; [[-]]  
5           a code generator circuit [[(30)]] for generating a  
6     re-generated user code; [[-]]  
7           a device [[(24)]] for the estimation of a channel delay  
8     profile energy, for computing the time delays and amplitudes of  
9     each received multi-path component of said input signal  
10    [[(Y(k))]]; [[-]]  
11          a plurality of fingers [[(18)]]; [[-]] and  
12          a finger allocation unit [[(26)]] for processing said  
13    channel delay profile energy in order to select the strongest  
14    multi-path components of said input signal [[(y(k))]] and allocate  
15    them to said fingers [[(18)]]; ~~characterized in that said~~  
16    wherein the device [[(24)]] for the estimation of a channel delay  
17    profile energy comprises: [[-]]  
18          a basic correlator [[(32)]] having a first input [[(41)]]  
19    for sequentially reading from a memory location of said input  
20    memory buffer [[(16)]] a plurality of samples of said input signal  
21    [[(y(k))]], a second input [[(43)]] for receiving from said code  
22    generator circuit [[(30)]] a regenerated user code, and an output  
23    terminal for generating, by means of a correlation operation

24 between said plurality of samples of said input signal and said  
25 regenerated user code, a value of said channel delay profile energy  
26  $[(DP(1))]$ ;  $[[-]]$  and

27 a memory controller circuit  $[(36)]$  for addressing said  
28 input memory buffer  $[(16)]$  so that said first input  $[(41)]$  of  
29 said basic correlator  $[(32)]$  is successively fed with the content  
30 of the memory locations of said memory buffer  $[(16)]$ , each  
31 addressing operation corresponding to a new correlation operation  
32 of said basic correlator  $[(32)]$  for the computation of a new  
33 value of said channel delay profile energy  $[(DP(1))]$ .

1 2. (currently amended) The  $[A]$  receiver according to  
2 claim 1, wherein the values of said channel delay profile energy  
3  $[(DP(1))]$  are progressively stored in a profile accumulation  
4 memory  $[(34)]$ .

1 3. (currently amended) The  $[A]$  receiver according to  
2 claim 2, wherein said memory controller circuit  $[(36)]$  addresses  
3 said profile accumulation memory  $[(34)]$  so that the reading  
4 operations of said basic correlator  $[(32)]$  from said input memory  
5 buffer  $[(16)]$  and the writing operations into said profile  
6 accumulation memory  $[(34)]$  are handled by the memory controller  
7 circuit  $[(36)]$ .

1                   4. (currently amended) The [[A]] receiver according to  
2 claim 3, wherein said memory controller circuit [[(36)]] updates  
3 the addressing of said input memory buffer [[(16)]] and said  
4 profile accumulation memory [[(34)]] every NC chips, where NC is  
5 equal to the integration window size, changing the reading and  
6 writing positions of said basic correlator [[(32)]].

1                   5. (currently amended) The [[A]] receiver according to  
2 claim 3, wherein, when the last memory location of both said input  
3 memory buffer [[(16)]] and said profile accumulation memory  
4 [[(34)]] is reached, the addressing restarts circularly on a first  
5 location of both memories [[(16, 34)]].

1                   6. (currently amended) The [[A]] receiver according to  
2 claim 3, wherein said basic correlator [[(32)]] is time  
3 multiplexed, at a multiple of the chip frequency [[( $F_c$ )]], between  
4 a plurality of memory locations of said input memory buffer  
5 [[(16)]] and of said profile accumulation memory [[(34)]].

1                   7. (currently amended) The [[A]] receiver according to  
2 claim 2, wherein said delay profile energy [[( $DP_{acc}(1)$ )]] is  
3 obtained by accumulating the energies [[( $DP_i(1)$ )]] of several delay  
4 profiles.

1           8. (currently amended) A method for the estimation of  
2 the channel delay profile energy in a spread spectrum digital  
3 communication receiver of the type comprising an input memory  
4 buffer  $[(16)]$  for storing samples of an input signal  $[(y(k))]$   
5 and a code generator circuit  $[(30)]$  for generating a re-generated  
6 user code, the method comprising the steps of:

7           a) sequentially reading a first plurality of samples of  
8 the input signal  $y(k)$  from said memory buffer 16;

9           b) correlating said plurality of samples of said input  
10 signal with said regenerated user code for generating a first value  
11 of the channel delay profile energy  $[(DP(k))]$ ;

12           c) updating the reading position on said input memory  
13 buffer  $[(16)]$  for reading a further plurality of samples of the  
14 input signal  $[(y(k))]$ ;

15           d) correlating said further plurality of samples of said  
16 input signal with said regenerated user code for generating a  
17 further value of the channel delay profile energy  $[(DP(k+1))]$ ,  
18 said generated value of the channel delay profile energy  
19  $[(DP(k+1))]$  being stored in a profile accumulation memory  
20  $[(34)]$ ; and

21           e) repeating the steps c)] to d)] in order to compute  
22 all the values of the channel delay profile.

1                   9. (currently amended) The [[A]] method according to  
2 claim 8, further comprising the step of  
3                   storing each generated value of said channel delay  
4 profile energy [[(DP(1))]] in a profile accumulation memory  
5 [[(34)]].

1                   10. (currently amended) A spread spectrum digital  
2 communication receiver, the receiver comprising: [[-]]  
3                   a code generator circuit [[(52)]] for generating a  
4 re-generated user code; [[-]]  
5                   a memory buffer [[(50)]] for storing samples of said  
6 re-generated user code; [[-]]  
7                   a device [[(64)]] for the estimation of a channel delay  
8 profile energy, for computing the time delays and amplitudes of  
9 each received multi-path component of an input signal [[(y(k))]]  
10 received by said receiver; [[-]]  
11                   a plurality of fingers [[(78)]]; [[-]] and  
12                   a finger allocation unit [[(76)]] for processing said  
13 channel delay profile energy in order to select the strongest  
14 multi-path components of said input signal [[(y(k))]] and allocate  
15 them to said fingers [[(78)]]; ~~characterized in that said~~  
16 wherein the device [[(64)]] for the estimation of a channel delay  
17 profile energy comprises: [[-]]  
18                   a basic correlator [[(54)]] having a first input [[(41)]]  
19 for receiving said input signal [[(y(k))]] and a second input

20     [[43]] for sequentially reading from a memory location of said  
21     memory buffer [[50]] a plurality of samples of said re-generated  
22     user code, and an output terminal for generating, by means of a  
23     correlation operation between said input signal and said plurality  
24     of samples of said regenerated user code, a value of said channel  
25     delay profile energy [[DP(1)]]; [-] and

26             a memory controller circuit [[58]] for addressing said  
27     memory buffer [[50]] so that said second input [[43]] of said  
28     basic correlator [[54]] is successively fed with the content of  
29     the memory locations of said memory buffer [[50]], each  
30     addressing operation corresponding to a new correlation operation  
31     of said basic correlator [[58]] for the computation of a new  
32     value of said channel delay profile energy [[DP(1)]].

1             11. (currently amended) The [[A]] receiver according to  
2     claim 10, wherein the values of said channel delay profile energy  
3     [[DP(1)]] are progressively stored in a profile accumulation  
4     memory [[56]].

1           12. (currently amended) The [[A]] receiver according to  
2 claim 11, wherein said memory controller circuit [[(58)]] addresses  
3 said profile accumulation memory [[(56)]] so that the reading  
4 operations of said basic correlator [[(54)]] from said memory  
5 buffer [[(50)]] and the writing operations into said profile  
6 accumulation memory [[(56)]] are handled by the memory controller  
7 circuit [[(58)]].

1           13. (currently amended) The [[A]] receiver according to  
2 claim 12, wherein said memory controller circuit [[(58)]] updates  
3 the addressing of said memory buffer [[(50)]] and said profile  
4 accumulation memory [[(56)]] every NC chips, where NC is the  
5 integration window size, changing the reading and writing positions  
6 of said basic correlator [[(54)]].

1           14. (currently amended) The [[A]] receiver according to  
2 claim 12, wherein, when the last memory location of both said  
3 memory buffer [[(50)]] and said profile accumulation memory  
4 [[(56)]] is reached, the addressing restarts circularly on a first  
5 location of both memories [[(50, 56)]].

1           15. (currently amended) The [[A]] receiver according to  
2 claim 12, wherein said basic correlator [[(54)]] is time  
3 multiplexed, at a multiple of the chip frequency [[ $F_c$ ]], between  
4 a plurality of memory locations of said memory buffer [[(50)]] and  
5 of said profile accumulation memory [[(56)]].

1           16. (currently amended) The [[A]] receiver according to  
2 claim 12, wherein said delay profile energy [[ $(DP_{acc}(1))$ ]] is  
3 obtained by accumulating the energies [[ $(DP_i(1))$ ]] of several delay  
4 profiles.

1           17. (currently amended) A method for the estimation of  
2 the channel delay profile energy in a spread spectrum digital  
3 communication receiver of the type comprising a code generator  
4 circuit [[(52)]] for generating a re-generated user code and a  
5 memory buffer [[(50)]] for storing samples of said re-generated  
6 user code, comprising the steps of:

7           a) sequentially reading a first plurality of samples of  
8 the re-generated user code from said memory buffer [[(50)]];

9           b) correlating said plurality of samples of said  
10 re-generated user code with an input signal  $y(k)$  for generating a  
11 first value of the channel delay profile energy [[ $(DP(k))$ ]];

12           c) updating the reading position on said input memory  
13 buffer [[(50)]] for reading a further plurality of samples of the  
14 re-generated user code;



15           d) correlating said further plurality of samples of said  
16 re-generated user code with said input signal  $[[y(k)]]$  for  
17 generating a further value of the channel delay profile energy  
18  $[[DP(k+1)]]$ , said generated value of the channel delay profile  
19 energy  $[[DP(k+1)]]$  being stored in a profile accumulation memory  
20  $[[56)]]$ ; and  
21           e) repeating the steps c)] to d)] in order to compute  
22 all the values of the channel delay profile.

1           18. (currently amended) The  $[[A]]$  method according to  
2 claim 17, further comprising the step of storing each generated  
3 value of said channel delay profile energy  $[[DP(1)]]$  in a profile  
4 accumulation memory  $[[56)]]$ .